IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a power supply node;

a load circuit;

a transistor coupled between the power supply node and the load circuit; and

a control circuit to utilize the transistor as a regulator or a sleep transistor, wherein the control circuit is coupled to provide either a first signal to influence operation of the transistor as a sleep transistor or a second signal to influence operation of the transistor as a regulator.

2. (Original) The apparatus of claim 1 wherein the control circuit includes an error amplifier to influence operation of the transistor.

3. (Original) The apparatus of claim 1 wherein the control circuit comprises a plurality of control loops to influence operation of the transistor as a regulator.

4. (Original) The apparatus of claim 3 wherein the control circuit comprises a first control loop having an error amplifier.

5. (Original) The apparatus of claim 4 wherein the control circuit further comprises a second control loop having a higher bandwidth than the first control loop.

6. (Original) The apparatus of claim 5 wherein the second control loop is adapted to sense a voltage between the transistor and the load circuit using a source of a second transistor.

7. (Original) The apparatus of claim 1 further comprising:

a second power supply node; and

a second transistor coupled between the load circuit and the second power supply node;

wherein the control circuit is adapted to utilize the second transistor as a regulator or a sleep transistor.

8. (Original) The apparatus of claim 1 wherein the load circuit comprises a memory circuit.

9. (Original) The apparatus of claim 1 wherein the load circuit comprises a cache memory circuit.

10. (Currently Amended) A circuit comprising:

a sleep transistor coupled between a power supply node and a load circuit, wherein the sleep transistor is coupled to provide power supply regulation[[.]];

an error amplifier coupled to the sleep transistor; and

a multiplexer coupled between the error amplifier and the sleep transistor, wherein the multiplexer is adapted to conditionally turn off the sleep transistor.

Claims 11-13 (Canceled)

14. (Currently Amended) The circuit of claim ~~13~~ 10 ~~wherein the control circuit comprises~~ further comprising a first control loop ~~including an~~ that includes the error amplifier.

15. (Currently Amended) The circuit of claim 14 ~~wherein the control circuit comprises~~ further comprising a second control loop including a sensing transistor coupled to sense a voltage variation using a source terminal.

16. (Currently Amended) The circuit of claim 15 ~~wherein the control circuit further comprises~~ further comprising a bias transistor coupled between the sensing transistor and a second power supply node.

17. (Original) The circuit of claim 16 further comprising a voltage divider coupled between the power supply node and a node formed at a junction between the sensing transistor and bias transistor, the voltage divider to influence operation of the sleep transistor.

18. (Original) The circuit of claim 10 wherein the load circuit comprises a memory circuit.

19. (Original) The circuit of claim 10 wherein the load circuit comprises a cache memory circuit.

20. (Original) The circuit of claim 10 wherein the load circuit is in a first integrated circuit die, and the sleep transistor is in a second integrated circuit die.

21. (Original) The circuit of claim 20 wherein the first integrated circuit die is mounted on top of the second integrated circuit die.

22. (Currently Amended) A method comprising performing power supply regulation using a sleep transistor[[.]] and sensing a voltage and influencing operation of the sleep transistor with an amplifier in a first control loop.

23. (Original) The method of claim 22 further comprising turning off the sleep transistor.

24. (Canceled)

25. (Currently Amended) The method of claim ~~24~~ 22 further comprising sensing the voltage and influencing the operation of the sleep transistor in a second control loop.

26. (Currently Amended) An electronic system comprising:

a first integrated circuit including a sleep transistor coupled between a power supply node and a load circuit, and an error amplifier coupled to the sleep transistor, the sleep transistor to provide power supply regulation; and

a static random access memory device coupled to the first integrated circuit.

27. (Original) The electronic system of claim 26 wherein the first integrated circuit further includes an error amplifier coupled to the sleep transistor.

28. (Original) The electronic system of claim 27 wherein the first integrated circuit further includes a multiplexer coupled between the error amplifier and the sleep transistor, wherein the multiplexer is adapted to conditionally turn off the sleep transistor.

29. (Original) The electronic system of claim 26 wherein the first integrated circuit further includes a control circuit to conditionally turn off the sleep transistor.

30. (Original) The electronic system of claim 29 wherein the control circuit comprises a first control loop including an error amplifier.